THAT WHICH IS CLAIMED IS:

1. An integrated circuit device comprising:

an integrated circuit substrate;

a capacitor on the integrated circuit substrate, the capacitor including a lower electrode, a dielectric layer on the lower electrode and an upper electrode on the dielectric layer; and

a barrier layer between the dielectric layer and the upper electrode, the barrier layer including titanium oxide and the dielectric layer including tantalum oxide and/or hafnium oxide.

2. The integrated circuit device of Claim 1, wherein the upper electrode comprises a noble metal.

3. The integrated circuit device of Claim 3, wherein the dielectric layer has a thickness of from about 20 Å to about 50 Å.

4. The integrated circuit device of Claim 1, wherein the barrier layer has a thickness of from about 10 Å to about 50 Å.

5. The integrated circuit device of Claim 1, wherein the lower electrode comprises at least one of a doped polysilicon layer, a noble metal layer and a noble metal oxide layer.

6. The integrated circuit device of Claim 1, wherein the upper electrode comprises at least one of Ruthenium (Ru), Platinum (Pt), Iridium (Ir), Ru oxide, Pt oxide and Ir oxide.

7. A method of forming an integrated circuit device comprising:

forming a lower electrode of a capacitor on an integrated circuit substrate;

forming a dielectric layer on the lower electrode, the dielectric layer including tantalum oxide and/or hafnium oxide;

forming a barrier layer on the dielectric layer and the upper electrode, the barrier layer including a titanium oxide layer; and

forming an upper electrode on the dielectric layer.

8. The method of Claim 7, wherein forming the barrier layer and the upper electrode further comprise:

forming the titanium oxide layer on the dielectric layer;

thermally treating the dielectric layer and the titanium oxide layer; and

forming an upper electrode on the titanium oxide layer, the upper electrode including a noble metal.

9. The method of Claim 7, wherein forming the dielectric layer comprises forming a tantalum oxide layer on the lower electrode by chemical vapor deposition (CVD).

10. The method of Claim 7, wherein forming the dielectric layer comprises forming a hafnium oxide layer on the lower electrode by atomic layer deposition (ALD).

11. The method of Claim 7, wherein forming the dielectric layer comprises forming the dielectric layer having a thickness of from about 20 Å to about 50 Å.

12. The method of Claim 8, wherein forming the titanium oxide layer comprises forming the titanium oxide layer by atomic layer deposition (ALD).

13. The method of claim 12, wherein forming the titanium oxide layer further comprises:

supplying a titanium source to an upper portion of the dielectric layer in a chamber;

purging an inside of the chamber;

supplying an oxidizer;

purging the inside of the chamber; and

repeating the supplying a titanium source, purging, supplying an oxidizer and the purging at least once.

14. The method of Claim 12, wherein forming the titanium oxide layer comprises forming the titanium oxide layer to have a thickness of from about 10 Å to about 50 Å.

15. The method of Claim 7, wherein forming the lower electrode comprises forming the lower electrode of at least one of a doped polysilicon layer, a noble metal layer, and a noble metal oxide layer.

16. The method of Claim 7 wherein forming the upper electrode comprises forming the upper electrode of at least one of Ruthenium (Ru), Platinum (Pt), Iridium (Ir), Ru oxide, Pt oxide and Ir oxide.

17. The method of Claim 8, wherein the thermally treating comprises thermally treating the dielectric layer and the titanium oxide layer at a temperature lower than a crystallization temperature of the dielectric layer.

18. The method of Claim 8, wherein forming the upper electrode is followed by curing the resultant structure in an oxygen atmosphere at a temperature of from about 350 °C to about 450 °C.

19. A method of fabricating an integrated circuit device, the method comprising:

forming a lower electrode on an integrated circuit substrate;

depositing a tantalum oxide layer on the lower electrode;

depositing a titanium oxide layer for a barrier layer on the tantalum oxide layer by atomic layer deposition (ALD);

thermally treating the titanium oxide layer and the tantalum oxide layer;

forming an upper electrode including Ruthenium (Ru) on the titanium oxide layer; and

curing the upper electrode.

20. A method of fabricating an integrated circuit device, the method comprising:

forming a lower electrode on an integrated circuit substrate;

depositing a hafnium oxide layer on the lower electrode;

depositing a titanium oxide layer for a barrier layer on the hafnium oxide layer;

thermally treating the titanium oxide layer and the hafnium oxide layer;

forming an upper electrode of Ruthenium (Ru) on the titanium oxide layer; and

curing the resultant structure.